In the Claims:

1-13. (Canceled)

14. (Original) A resistor pattern for an integrated circuit memory device having a capacitor, comprising:

an integrated circuit substrate;

a low resistive layer formed on the integrated circuit substrate, the low resistive layer defining an upper capacitor electrode of the capacitor and defining a low resistive layer of the resistor pattern in a region of the integrated circuit substrate displaced from the upper capacitor electrode;

an insulating layer formed on the upper capacitor electrode and the low resistive layer of the resistor pattern; and

a high resistive layer formed on the insulating layer, the low resistive layer, the insulating layer and the high resistive layer defining the resistor pattern in the region of the integrated circuit substrate displaced from the upper capacitor electrode.

15. (Original) The resistor pattern of Claim 14 wherein the low resistive layer comprises a material having a specific resistance of at least a hundred $\mu\Omega\bullet$cm.

16. (Original) The resistor pattern of Claim 15 wherein the low resistive layer comprises at least one of Ru, Pt, RuO_2, Ir, IrO_2, W, Al, Cu, TiN, TaN, and/or WN.

17. (Original) The resistor pattern of Claim 14 wherein the insulating layer comprises at least one of SiO_2, Ta_2O_5, Al_2O_3, and/or Si_3N_4.

18. (Original) The resistor pattern of Claim 14 wherein the high resistive layer has a specific resistance of at least a hundred $\mu\Omega\bullet$cm.

19. (Original) The resistor pattern of Claim 18 wherein the high resistive layer has a specific resistance of at least a thousand $\mu\Omega\bullet$cm.

20. (Original) The resistor pattern of Claim 18 wherein the high resistive layer comprises a doped polysilicon layer.

21. (Original) The resistor pattern of Claim 14 further comprising, a TiN layer formed between the low resistive layer and the insulating layer.

22-32. (Canceled)